

**National University**



of Computer



and



Emerging Sciences



Chiniot



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Faisalabad Campus



**EE1005 – Digital Logic Design**

**Quiz# 5**

**Instructor:** Muhammad Adeel Tahir **Section:** CS-2F **Time:** 40 Minutes

**Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

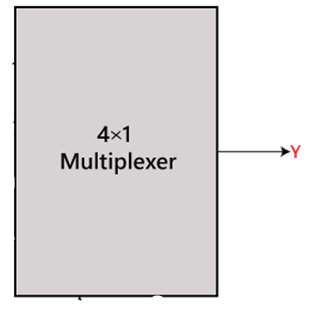
**Roll No: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Total: 65 marks**

***Instructions:*** *Make sure the handwriting is neat and clean while drawing the circuit, quiz will be marked as 0 if attempted in a writing that is not readable at all.*

**PART (a)**

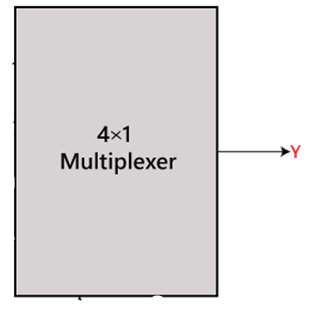
**Question 1:** Design a circuit that takes a 3-bit binary input and outputs a 2-bit binary number representing the count of '1's in the input. Use a 3-to-8 decoder, OR gates, and a 4-to-2 encoder for implementation. **[5 marks]**

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**Question 2**: Implement the following Boolean function with 4X1 MUX and external gates where AB are select lines and C D are data lines. **[10+10 marks =20 marks]**

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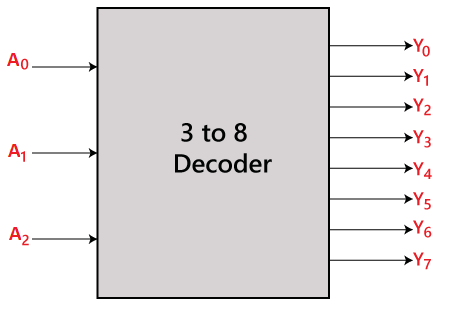
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**Question 3:** Design a combinational circuit with a decoder to accept a 3-bit number and generate the output binary number equal to the square of the input number. Implement this using 8:4 decoder. **[15 marks]**

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**Working (if any):**

**(No cutting allowed)**



**PART (B)**

**Question 4:** A sequential circuit with two D flip-flops A and B, two inputs, x and y ; and one output z is specified

by the following next-state and output equations. **[15 Marks]**

Implement the following:

1. Draw the logic diagram of the circuit. **5 marks**
2. List the state table for the sequential circuit. **6 marks**
3. Draw the corresponding state diagram. **4 marks**

**Logic Diagram of the circuit (diagram must be neat and clean with proper connections, a 0 will be awarded in case the connections are not labelled and drawn properly)**

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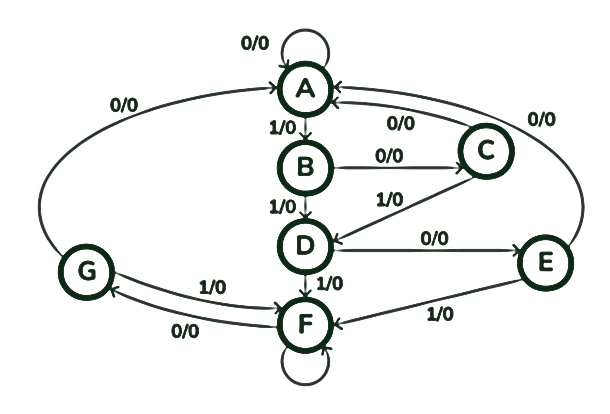
**State Diagram (No cutting allowed)**

**Question 5:** Given the following state diagram, perform the following tasks: **[5+5+5=15 marks]**

a) Construct the state table that corresponds to the given state diagram.

b) Reduce the state table to its minimized form step by step.

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| **State Table (binary checking- no cutting allowed)** | | | | |
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c) Draw the reduced state diagram

**a)**